REMARKS

Claims 1, 3, 7 and 9, as amended, remain herein. Claims 2, 4-6, 8 and 10-41 remain herein but are presently withdrawn from consideration.

Claim 1 has been amended to recite a liquid crystal device including signal lines and thin-film transistors for performing a pseudo dot inversion which changes the polarity of a pixel on a per image-signal-line basis. See applicants' specification, page 14, second full paragraph, and page 18, line 9 to page 20, line 6, wherein two of the thin-film transistors located between an adjacent two of the image signal lines have respective source electrodes connected to different image signal lines and respective drain electrodes connected to respective pixel electrodes. See applicants' Fig. 8, showing two TFTs 101 and 102 located between two neighboring image signal lines 21 and 22, wherein source electrodes 71 and 72 are connected to different image signal lines 21 and 22, and drain electrodes 81 and 82 are connected to respective pixel electrodes 61 and 62.

1. The finality of the restriction requirement is acknowledged.

1. Claims 1 and 3 were rejected under 35 U.S.C. §102(b) over Japanese Patent Publication JP 08-240811.

The presently claimed liquid crystal device includes signal lines and thin-film transistors for performing a pseudo dot inversion which changes the polarity of a pixel on a per image-signal-line basis, and includes a plurality of scan signal lines and image signal lines located orthogonally on a substrate with thin-film transistors in sections enclosed by scan and image signal lines and having alignment-shift-compensated electrodes and connections, wherein two of the thin-film transistors located between an adjacent two of the image signal lines have respective source electrodes connected to different image signal lines and respective drain electrodes connected to respective pixel electrodes. This arrangement is nowhere disclosed or suggested in the cited reference.

The Office Action cites JP '811 as allegedly disclosing a liquid crystal device having a plurality of scan signal lines and image signal lines located orthogonally on a substrate with thin-film transistors in sections enclosed by scan and image signal lines and having alignment-shift-compensated electrodes and connections. However, the JP '811 device is not for performing a pseudo dot inversion that changes the polarity of a pixel on a per image-signal-line basis. JP '811, paragraph 0033, describes the source electrode of thin film transistor 3 as connected to pixel electrodes 2R, 2G and 2B, and paragraph 0037 describes drain electrode d of thin film transistor 3 as connected to data line Ld. Such structure cannot perform a pseudo dot inversion as performed by the presently claimed invention. Please see the attached machine translation of JP '811.

In contrast, the presently claimed invention includes two of the thin-film transistors located between an adjacent two of the image signal lines having respective source electrodes connected to different image signal lines, and respective drain

electrodes connected to respective pixel electrodes. See applicants' Fig. 8, as described herein.

In applicants' invention, the respective gate, source, and drain electrodes of the two thin-film transistors are alignment-shift-compensated electrodes for causing at least one of a capacitance between the gate and drain electrodes and a capacitance between the gate and source electrodes to be constant or to vary equally in each of the two transistors. This avoids a difference between the charging abilities of the adjacent pixels and each scan signal line, and non-uniform displays such as flickers or vertical/horizontal strings.

For the foregoing reasons, JP '811 fails to disclose all elements of applicants' claimed invention, and therefore is not a proper basis for rejection under §102. And, there is no disclosure or teaching in JP '811 that would have suggested the desirability of modifying any portions thereof effectively to anticipate or suggest applicants' presently claimed invention. Claim 3, which depends from claim 1, is allowable for the same reasons explained herein for claim 1. Accordingly,

reconsideration and withdrawal of this rejection are respectfully requested.

2. Claims 7 and 9 were rejected under 35 U.S.C. §103(a) over JP '811 and European Patent Application EP 0 453 324.

Claims 7 and 9, which depend from claim 1, are allowable for the same reasons explained herein for claim 1.

Moreover, the Office Action cites EP '324 as allegedly teaching variation in an overlapping area between the channel protective film and the source electrode responsive to an alignment shift being constant or equal. However, EP '324 does not provide the deficiency of JP '811 explained herein, i.e., the system of EP '324 does not perform a pseudo dot inversion that changes the polarity of a pixel on a per image-signal-line basis. Kondo 'EP 324, Fig. 1, describes source electrodes 69a, 59a, 69b and 59b connected to common image signal line 56, not to different image signal lines, as required by the presently claimed invention.

For the foregoing reasons, neither JP '811 nor EP '324 contains any teaching, suggestion, reason, motivation or incentive that would have led one of ordinary skill in the art to applicants' claimed invention. Nor is there any disclosure or teaching in either of these references that would have suggested the desirability of combining any portions thereof effectively to anticipate or suggest applicants' presently claimed invention. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

All claims 1, 3, 7 and 9 are now proper in form and patentably distinguished over all grounds of rejection stated in the Office Action. Accordingly, allowance of all claims 1, 3, 7 and 9 is respectfully requested.

Should the Examiner deem that any further action by the applicants would be desirable to place this application in even better condition for issue, the Examiner is requested to telephone applicants' undersigned representatives.

Respectfully submitted,

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December 7, 2004
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RWP:RNW/mhs

Attachment: Machine Translation of Teruhira JP '811

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ATTACHMENT A

TERUHIRA JP 08-240811

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the thin film transistor panel (henceforth the TFT panel) used for an active-matrix liquid crystal display component.
[0002]
[Description of the Prior Art] The active-matrix liquid crystal display component which uses a thin film transistor (TFT) as an active element The TFT panel which prepared transparence radical Sakagami a pixel electrode group, two or more gate lines and a data line, and two or more thin film transistors that correspond to each pixel electrode, respectively, With the liquid crystal display component which is what enclosed liquid crystal and displays multicolor color pictures, such as a full color image, between the opposite panels which prepared transparence radical Sakagami the counterelectrode which counters said pixel electrode group The opposite panel or the TFT panel was made equivalent to each pixel electrode, and the light filter of red, green, and blue is prepared.
[0003] By the way, there are various methods in the array pattern of the pixel in the above-mentioned active-matrix liquid crystal display component, and there are some which display a pixel by the mosaic-like array pattern as the one method.
[0004] This method is mainly adopted as the liquid crystal display component which displays a multicolor color or a full color image, and red, green, and the liquid crystal display component of the method which displays a blue pixel by the mosaic-like array pattern have the advantage that the good color of color mixture can be expressed.
[0005] The TFT panel used for the above-mentioned red, green, and the active-matrix liquid crystal display component of the method which displays a blue pixel by the mosaic-like array pattern is conventionally considered as the following configurations. Drawing 4 is some top views of the conventional TFT panel. In addition, this TFT panel is used for the liquid crystal display component which has prepared the light filter of red, green, and blue at the opposite panel.
[0006] The pixel electrode group which arranged two or more pixel electrodes 2R and 2G and 2B in the line writing direction (it sets to drawing and is a longitudinal direction), and the direction of a train (it sets to drawing and is a lengthwise direction) on the transparence substrate 1 with which this TFT panel consists of glass etc., Two or more thin film transistors 3 connected to each pixel electrode of this pixel electrode group, respectively, Two or more gate lines Lg which are made to correspond to each pixel electrode line of said pixel electrode group, respectively, and it wires, and **** a gate signal to said thin film transistor 3, Two or more data lines Ld which are made to correspond to each pixel electrode train of said pixel electrode group, respectively, and it wires, and supply a data signal to said thin film transistor 3 are formed.
[0007] First, explanation of a pixel electrode group forms each pixel electrodes 2R and 2G of this pixel electrode group, and 2B by transparence electric conduction film, such as ITO. A pixel electrode for 2R to display a red pixel among these pixel electrodes 2R and 2G and 2B (electrode with which the red light filter by the side of an opposite panel corresponds), A pixel electrode for 2G to display a green pixel (electrode with which the green light filter by the side of an opposite panel corresponds), 2B is a pixel electrode (electrode with which the blue light filter

by the side of an opposite panel corresponds) for displaying a blue pixel. These pixel electrodes 2R and 2G and 2B To a line writing direction (it sets to drawing and is a longitudinal direction), it arranges by turns, and is arranged in the shape of a straight line. In the direction of a train It shifts about 1.5 pitches of pixel electrodes for displaying the pixel of the same color, i.e., the pixel electrodes corresponding to the same data line Ld, at a time by turns for every line in an one direction and the other directions (it sets to drawing and they are the left and the right), and is arranged by zigzag.

[0008] Moreover, the thin film transistor 3 corresponding to each pixel electrodes 2R and 2G of the above-mentioned pixel electrode group, and 2B, respectively The gate dielectric film 4 which consists of a wrap SiN (silicon nitride) etc. the gate electrode g formed on the substrate 1, and this gate electrode g, The i-type semiconductor film 5 which consists of a-Si (amorphous silicon) which was made to counter with said gate electrode g, and was formed on this gate dielectric film 4, It consists of a source electrode s formed through the n-type-semiconductor film (not shown) which consists of a-Si which doped n mold impurity on this i-type semiconductor film 5, and a drain electrode d.

[0009] On the other hand, the gate line Lg corresponding to each pixel electrode line of the above-mentioned pixel electrode group is made to meet said pixel electrode line, and is wired on the substrate 1, the gate electrode g of each thin film transistor 3 is made to jut out over said gate line Lg at the 1 side, and is formed in one, and the source electrode s and the drain electrode d are arranged in the direction along the gate line Lg, respectively.

[0010] moreover, the gate dielectric film 4 of the above-mentioned thin film transistor 3 — the gate line Lg — covering — a substrate 1 — it is mostly formed in the whole surface, and each pixel electrodes 2R and 2G and 2B are formed on said gate dielectric film 4, and are connected to the source electrode s of said thin film transistor 3 in the green section.

[0011] On the other hand, the data line Ld corresponding to each pixel electrode train for displaying the pixel of the same color of the above-mentioned pixel electrode group is made to correspond to the pixel electrode train arranged at zigzag on the interlayer insulation film (not shown) which consists of SiN formed on the above-mentioned gate dielectric film 4, meandering wiring is carried out, respectively, and this data line Ld is connected to the drain electrode d of the above-mentioned thin film transistor 3 in the contact hole prepared in said interlayer insulation film.

[0012] If the wiring condition of this data line Ld is explained about the data line corresponding to the pixel electrode train for displaying a red pixel, this data line Ld makes it meet the right side edge of pixel electrode 2R which has shifted leftward among each pixel electrode 2R arranged to zigzag, and the left side edge of pixel electrode 2R which has shifted rightward, and meandering wiring is carried out. That is, this data line Ld is wired so that the **** line section Ldy which meets in the direction of a train, and the infestation line section Ldx crooked along with a line writing direction from this **** line section Ldy may continue by turns.

[0013] In addition, a data line Ld is made to meet the left side edge of pixel electrode 2R which has shifted rightward [of pixel electrode 2R shifted leftward / the right side edge and rightward], and it is wiring for shortening the die length of the infestation line section Ldx in alignment with a line writing direction, and simplifying leading about of a data line Ld.

[0014] However, if a data line Ld is wired as mentioned above, the location of the data line Ld to the thin film transistor 3 corresponding to pixel electrode 2R shifted leftward and the location of the data line Ld to the thin film transistor 3 corresponding to pixel electrode 2R which has shifted rightward will become reverse mutually.

[0015] So, by this TFT panel, physical relationship of the source of the thin film transistor 3 corresponding to pixel electrode 2R shifted leftward and the thin film transistor 3 corresponding to pixel electrode 2R which has shifted rightward, and the drain electrodes s and d was mutually made into reverse, pixel electrode 2R was connected to the source electrode s of these thin film transistors 3, and the data line Ld is connected to the drain electrode d.

[0016] The wiring condition of the above-mentioned data line Ld is the same also in the data line corresponding to the pixel electrode train for displaying the data line and blue pixel corresponding to a pixel electrode train for displaying a green pixel. Moreover, the thin film

transistor 3 corresponding to pixel electrode 2G for displaying a green pixel The thin film transistor 3 corresponding to pixel electrode 2B for displaying a blue pixel Physical relationship of the source and drain electrode s-d was mutually made into reverse by the thing corresponding to the pixel electrode which has shifted rightward [a thing and rightward] corresponding to the pixel electrode shifted leftward, pixel electrode 2G and 2B were connected to the source electrode s, and the data line Ld is connected to the drain electrode d.
[0017] Moreover, the infestation line section Ldx of the above-mentioned data line Ld avoids the above-mentioned gate line Lg top, and is wired in the side, and each pixel electrodes 2R and 2G and 2B secure the wiring tooth space of the **** line section Ldy of a data line Ld between the train, secure two wiring tooth spaces of the infestation line section Ldx of a data line Ld, and the gate line Lg to space, and are arranged.
[0018] Moreover, in drawing 4 , Lc is a capacitor line which constitutes the compensation capacitance (storage capacitor) for holding the potential of each pixel electrodes 2R and 2G and 2B, and this capacitor line Lc is made to correspond to each pixel electrode line, respectively, and is wired.
[0019] This capacitor line Lc makes the pixel electrodes 2R and 2G of each line, and the end edge (the wiring side of the gate line Lg is the edge of an opposite hand) of 2B counter on a substrate 1, and is wired, and the above-mentioned compensation capacitance consists of pixel electrodes 2R and 2G, 2B and said capacitor line Lc, and gate dielectric film 4 in the meantime.
[0020] In addition, by the TFT panel shown in drawing 4 , in order to form the compensation capacitance of sufficient capacity value, the lobe which counters the pixel electrodes 2R and 2G and the edges-on-both-sides section of 2B is formed in the capacitor line Lc, and the opposed face product of the capacitor line Lc, and the pixel electrodes 2R and 2G and 2B is enlarged.
[0021] Moreover, although the above-mentioned capacitor line Lc is generally formed by the same opaque metal membrane as the gate electrode g of a thin film transistor 3, and the gate line Lg, this capacitor line Lc may be formed by transparence electric conduction film, such as ITO.
[0022]
[Problem(s) to be Solved by the Invention] However, by the above-mentioned conventional TFT panel, a data line Ld is made to meet the right side edge of pixel electrode 2R which has shifted leftward among each pixel electrode 2R arranged to zigzag so that leading about may become it is short and easy as much as possible, and the left side edge of pixel electrode 2R which has shifted rightward, and meandering wiring has been carried out. And it arranges so that each thin film transistor 3 corresponding to these pixel electrode 2R may be stood in a line in the direction in which the source electrode s and the drain electrode d are along the gate line Lg. Therefore, it will become reverse mutually by the case where it is located in the case where each pixel electrode 2R to which arrangement of the source electrode s in each thin film transistor 3 and the drain electrode d corresponds is located in the left-hand side of the **** line Ldy of a data line Ld, and right-hand side. For this reason, when an alignment gap occurs in the direction which meets on the gate line Lg in a production process, property fluctuation of the thin film transistor accompanying it differs by the left-hand side thin film transistor and right-hand side thin film transistor corresponding to pixel electrode 2R of the same red, consequently also in the pixel of the same red, gradation differs and image quality deteriorates remarkably.
[0023] Making it correspond to the pixel electrode train which arranged each pixel electrode corresponding to the same data line to zigzag, and has arranged said data line to zigzag, and carrying out meandering wiring, even if it changes the property of a thin film transistor by the alignment gap in a production process, the gradation of a color does not differ in the same color, but this invention aims at offering the TFT panel by which good color display is always obtained.
[0024]
[Means for Solving the Problem] The pixel electrode group to which the TFT panel of this invention arranged two or more pixel electrodes in the line writing direction and the direction of a train on the transparence substrate, Two or more thin film transistors which maintained predetermined spacing, installed the drain electrode and the source electrode, were formed through the semi-conductor layer on the gate electrode, and were connected to each pixel

electrode of said pixel electrode group through said source electrode, respectively, Two or more gate lines which are connected to the gate electrode of said thin film transistor which is made to correspond to each pixel electrode line of said pixel electrode group, respectively, and it wires, and corresponds, and supply a gate signal, It comes to form two or more data lines which are made to correspond to each pixel electrode train of said pixel electrode group, respectively, and it wires, and supply a data signal to said thin film transistor. And while making it correspond to the pixel electrode train which shifted each pixel electrode corresponding to the same data line by turns in an one direction and the other directions for every line, arranged it to zigzag, and has arranged said data line to zigzag and carrying out meandering wiring Each thin film transistor is arranged so that the side-by-side installation direction of a source electrode and a drain electrode may meet in said direction of a train. Make each thin film transistor correspond and two or more lobes which project along with said line writing direction in a data line are formed. It is characterized by connecting the drain electrode of each thin film transistor arranged through each lobe by each pixel electrode corresponding to a data line and this data line.

[0025] While arranging a thin film transistor in the TFT panel of this invention so that the side-by-side installation direction of a source electrode and a drain electrode may meet in the direction of a train Make each pixel electrode connected to this data line correspond, and the lobe which projects along with a line writing direction in a data line is formed. Since the drain electrode and data line of each thin film transistor which were arranged by the pixel electrode which corresponds through this lobe were connected Arrangement of the drain electrode d of all thin film transistors and the source electrode s can be arranged uniformly. By this Even if an alignment gap arises in a production process, property fluctuation of the thin film transistor by it becomes fixed by all thin film transistors, and generating of a poor display from which gradation differs by the same foreground color is prevented, and it becomes possible to always obtain good color display easily.

[0026]

[Embodiment of the Invention] Hereafter, one example of this invention is explained with reference to drawing 1 - drawing 3 about the TFT panel used for the active-matrix liquid crystal display component of the method which displays the pixel of red, green, and blue by the mosaic-like array pattern.

[0027] The expanded sectional view and drawing 3 to which drawing 1 meets some top views of the TFT panel, and drawing 2 meets the II-II line of drawing 1 are drawing 1 . III-III It is the expanded sectional view which meets a line. In addition, in drawing, a same sign is given to the thing corresponding to the conventional TFT panel shown in drawing 4 , and the explanation is omitted about the same part as the conventional TFT panel.

[0028] The pixel electrode group to which this TFT panel arranged two or more pixel electrodes 2R and 2G and 2B in the line writing direction and the direction of a train on the substrate 1, Each pixel electrodes 2R and 2G of this pixel electrode group, and two or more thin film transistors 3 connected to 2B, respectively, Two or more gate lines Lg which are made to correspond to each pixel electrode line of said pixel electrode group, respectively, and it wires, and supply a gate signal to said thin film transistor 3, Two or more data lines Ld which are made to correspond to each pixel electrode train of said pixel electrode group, respectively, and it wires, and **** a data signal to said thin film transistor 3, It is the thing in which said each pixel electrodes 2R and 2G and the capacitor line Lc which forms compensation capacitance between 2Bs were formed. Like the conventional TFT panel, it shifts each pixel electrodes 2R and 2G and 1.5 pitches of 2Bs at a time by turns in an one direction and the other directions for every line, and they are arranged by zigzag, and are wired like [the gate line Lg and the capacitor line Lc] the conventional TFT panel.

[0029] On the other hand, by this TFT panel, while making the thin film transistor 3 corresponding to each pixel electrodes 2R and 2G of the above-mentioned pixel electrode group, and 2B into the following structures, that infestation line section Ldx is made to counter up and down with the gate line Lg, and the data line Ld which is made to correspond to the pixel electrode train arranged to zigzag, and carries out meandering wiring is wired, respectively.

[0030] When the structure of the above-mentioned thin film transistor 3 is explained, first, this

thin film transistor 3 The gate electrode g which was made to **** on the above-mentioned gate line Lg at the - side, and was formed in one as shown in drawing 1 and drawing 3 The i-type semiconductor film 5 which consists of a-Si which this gate electrode g was made to counter with said gate electrode g on the gate dielectric film 4 which consists of a wrap SiN etc., and this gate dielectric film 4, and was formed, It consists of a source electrode s formed through the n-type-semiconductor film 6 which consists of a-Si which doped n mold impurity on this i-type semiconductor film 5, and a drain electrode d.

[0031] And in this TFT panel, the above-mentioned thin film transistor 3 is made into the structure formed in the sense from which 90 degrees of thin film transistors of the conventional TFT panel differ the source electrode s and the drain electrode d. that is <A To HREF="/Tokujitu/tjitemdrw.ipdl?N0000=239&N0500=1 E_N/;?7=;? 7>>///&N0001=126&N0552=9&N 0553= 000006" TARGET="tjitemdrw"> drawing 4 By the shown conventional TFT panel, although the source electrode s and the drain electrode d are made into the structure arranged in the direction along the gate line Lg, a thin film transistor 3 By the TFT panel of this example, the source electrode s of a thin film transistor 3 and the drain electrode d are arranged in the direction which intersects perpendicularly with the gate line Lg.

[0032] In addition, in drawing 1 and drawing 3 , although the gate electrode g of a thin film transistor 3 is greatly formed a little from the area of the i-type semiconductor film 5, even if the area of the gate electrode g is the same as the i-type semiconductor film 5, it is good, and may be made smaller than the i-type semiconductor film 5 in the range which does not become smaller than the channel field of the i-type semiconductor film 5.

[0033] moreover, the gate dielectric film 4 of the above-mentioned thin film transistor 3 — the conventional TFT panel — the same — the gate line Lg — covering — **** 1 — it is mostly formed in the whole surface, and each pixel electrodes 2R and 2G and 2B are formed on said gate dielectric film 4, and are connected to the source electrode s of said thin film transistor 3 at the edge.

[0034] When the wiring condition of the above-mentioned data line Ld is explained about the data line corresponding to the pixel electrode train for displaying a red pixel, next, this data line Ld In order to shorten the die length of the infestation line section Ldx and to simplify leading about of a data line Ld, the right side edge of pixel electrode 2R which has shifted leftward among each pixel electrode 2R arranged to zigzag, and the left side edge of pixel electrode 2R which has shifted rightward are made to meet, and meandering wiring is carried out. That is, this data line Ld is wired so that the **** line section Ldy which meets in the direction of a train, and the infestation line section Ldx crooked along with a line writing direction from this **** line section Ldy may continue by turns.

[0035] Thus, the location of the data line Ld to the thin film transistor 3 corresponding to pixel electrode 2R which has shifted leftward if a data line Ld is wired, Although the location of the data line Ld to the thin film transistor 3 corresponding to pixel electrode 2R shifted rightward will become reverse mutually Since Lobe Lda was formed, and the above-mentioned thin film transistor 3 is arranged by this TFT panel so that it may stand in a line in the direction in which the source electrode s and the gate line Lg and the drain electrode d cross at right angles, The physical relationship of the source of the thin film transistor 3 of each train and the drain electrodes s and d is arranged uniformly, and does not become reverse mutually like the conventional TFT panel.

[0036] The wiring condition of the above-mentioned data line Ld is the same also in the data line corresponding to the pixel electrode train for displaying the data line and blue pixel corresponding to a pixel electrode train for displaying a green pixel.

[0037] Moreover, each thin film transistor 3 is made to correspond to the above-mentioned data line Ld, respectively, Lobe Lda is formed in one and this data line Ld is connected to the drain electrode d of a thin film transistor 3 in said lobe Lda.

[0038] In addition, the data line Ld is wired on the interlayer insulation film 7 (it is omitting in drawing 1) which consists of SiN formed on the above-mentioned gate dielectric film 4, as shown in drawing 2 . A thin film transistor 3 is also covered, this interlayer insulation film 7 is formed, as shown not only in the wiring section of a data line Ld but in drawing 3 , and the lobe

Lda of a data line Ld is connected to the drain electrode d of a thin film transistor 3 in the contact hole 8 prepared in said interlayer insulation film 7.
[0039] And the infestation line section Ldx crooked along with the line writing direction of the above-mentioned data line Ld is wired by these gate line Lg and parallel right above the gate line Lg, and the insulator layer of the bilayer of the above-mentioned gate dielectric film 4 and an interlayer insulation film 7 insulates between the infestation line section Ldx of this data line Ld, and the gate line Lg.
[0040] That is, the above-mentioned TFT panel makes the infestation line section Ldx of this data line Ld counter up and down with the gate line Lg, and wires while it is made to correspond to the pixel electrode train which shifted each pixel electrodes 2R and 2G corresponding to the same data line Ld, and 2B by turns in an one direction and the other directions for every line, arranged them to zigzag, and has arranged said data line Ld to zigzag and carries out meandering wiring.
[0041] In this TFT panel, since the infestation line section Ldx of the data line Ld which carries out meandering wiring is made to counter up and down with the gate line Lg and it is wiring, each pixel electrodes 2R and 2G and the wiring tooth space secured to the space of 2B are good at one wiring. In addition, what is necessary is just to secure the wiring tooth space of the **** line section Ldy of a data line Ld like the conventional TFT panel between each pixel electrodes 2R and 2G and the train of 2B.
[0042] Therefore, according to the above-mentioned TFT panel, making it correspond to the pixel electrode train which arranged each pixel electrodes 2R and 2G corresponding to the same data line Ld, and 2B to zigzag, and has arranged said data line Ld to zigzag, and carrying out meandering wiring, area of the pixel electrodes 2R and 2G and 2B can be enlarged, and the numerical aperture of a liquid crystal display component can be raised.
[0043] However, by this TFT panel, since the infestation line section Ldx and the gate line Lg of a data line Ld have countered up and down through gate dielectric film 4 and an interlayer insulation film 7, parasitic capacitance is formed between the infestation line section Ldx of a data line Ld, and the gate line Lg, and this parasitic capacitance causes a voltage drop in the gate line Lg and a data line Ld.
[0044] In addition, also in the conventional TFT panel shown in drawing 4 , although the above-mentioned parasitic capacitance is formed in the intersection of the **** line section Ldy of a data line Ld, and the gate line Lg, since the infestation line section Ldx of a data line Ld has countered with the gate line Lg by the TFT panel of the above-mentioned example, the value of the parasitic capacitance formed between them is larger than the conventional TFT panel.
[0045] And since the electrical potential difference of the gate signal impressed to the gate line Lg is sufficiently high, Although the voltage drop in the gate line Lg hardly becomes a problem, since the data signal impressed to a data line Ld is a signal of the electrical potential difference according to image data, So that it will become close to the end side (it is an opposite hand to the impression side of a data signal) of a data line Ld, if the electrical potential difference of a data signal descends in a data line Ld The electrical potential difference of the data signal supplied to the pixel electrodes 2R and 2G and 2B through a thin film transistor 3 from a data line Ld becomes low, and display unevenness occurs for a liquid crystal display component.
[0046] However, if a data line Ld is formed with low resistance metals, such as aluminum (aluminum) and aluminum system alloy, the voltage drop in a data line Ld can be made small, and the good display which does not have display unevenness in a liquid crystal display component can be made to perform also in the TFT panel of the above-mentioned example.
[0047] Namely, although the amount of voltage drops in the overall length of the above-mentioned data line Ld is decided by the product of the resistance of this data line Ld, and the total value of the above-mentioned parasitic capacitance with which it is dotted on a data line Ld If a data line Ld is formed with low resistance metals, such as aluminum and aluminum system alloy Even if the value of the above-mentioned parasitic capacitance is large to some extent, the amount of voltage drops in a data line Ld can be made small (if the resistance of a data line Ld is 0, the amount of voltage drops in a data line Ld will be set to 0 irrespective of the value of parasitic capacitance by the theory top).

[0048] Especially the above-mentioned TFT panel fits the liquid crystal display component of an inside screen or a small screen. Moreover, in the case of the liquid crystal display component of an inside screen or a small screen Since the die length of a data line Ld is short, even if it forms this data line Ld with metals other than aluminum or aluminum system alloy, that resistance is small, and moreover, since there are few pixels Since there is few above-mentioned parasitic capacitance with which it is dotted on a data line Ld, the voltage drop in a data line Ld is small, therefore display unevenness does not generate it for a liquid crystal display component.
[0049] In addition, although considered as the structure arranged in the above-mentioned example in the direction which intersects perpendicularly the source electrode s and the drain electrode d with the gate line Lg in a thin film transistor 3, this thin film transistor 3 is good also as structure which has arranged the source electrode s and the drain electrode d in the direction along the gate line Lg like the thin film transistor 3 of the conventional TFT panel shown in drawing 4 .
[0050] Moreover, although the TFT panel of the above-mentioned example is used for the active-matrix liquid crystal display component of the method which displays the pixel of red, green, and blue by the mosaic-like array pattern If it is made to correspond to the pixel electrode train which this invention shifted each pixel electrode corresponding to the same data line by turns in an one direction and the other directions for every line, arranged it to zigzag, and has arranged said data line to zigzag and meandering wiring is carried out It is applicable also to the TFT panel used for the active-matrix liquid crystal display component of other methods.
[0051]
[Effect of the Invention] While according to the TFT panel of this invention arranging a thin film transistor so that the side-by-side installation direction of a source electrode and a drain electrode may meet in the direction of a train Make each pixel electrode connected to this data line correspond, and the lobe which projects along with a line writing direction in a data line is formed. Since the drain electrode and data line of each thin film transistor which were arranged by the pixel electrode which corresponds through this lobe were connected Arrangement of the drain electrode d of all thin film transistors and the source electrode s can be arranged uniformly. By this Even if an alignment gap arises in a production process, property fluctuation of the thin film transistor by it becomes fixed by all thin film transistors, and generating of a poor display from which gradation differs by the same foreground color is prevented, and it becomes possible to always obtain good color display easily.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Some top views of the TFT panel in which one example of this invention is shown.
[Drawing 2] The expanded sectional view which meets the II-II line of drawing 1 .
[Drawing 3] The expanded sectional view which meets the III-III line of drawing 1 .
[Drawing 4] Some top views of the conventional TFT panel.
[Description of Notations]
1 — Substrate
2R, 2G, 2B — Pixel electrode
3 — Thin film transistor
g — Gate electrode
4 — Gate dielectric film
5 — I-type semiconductor layer
6 — N-type-semiconductor layer
s — Source electrode
d — Drain electrode
Lg — Gate line
Lc — Capacitor line
7 — Interlayer insulation film
Ld — Data line
Ldx — Infestation line section

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The pixel electrode group which arranged two or more pixel electrodes in the line writing direction and the direction of a train on the transparence substrate, Two or more thin film transistors which maintained predetermined spacing, installed the drain electrode and the source electrode, were formed through the semi-conductor layer on the gate electrode, and were connected to each pixel electrode of said pixel electrode group through said source electrode, respectively, Two or more gate lines which are connected to the gate electrode of said thin film transistor which is made to correspond to each pixel electrode line of said pixel electrode group, respectively, and it wires, and corresponds, and supply a gate signal, It comes to form two or more data lines which are made to correspond to each pixel electrode train of said pixel electrode group, respectively, and it wires, and supply a data signal to said thin film transistor. And while making it correspond to the pixel electrode train which shifted each pixel electrode corresponding to the same data line by turns in an one direction and the other directions for every line, arranged it to zigzag, and has arranged said data line to zigzag and carrying out meandering wiring Each thin film transistor is arranged so that the side-by-side installation direction of a source electrode and a drain electrode may meet in said direction of a train. Make each thin film transistor correspond and two or more lobes which project along with said line writing direction in a data line are formed. The thin film transistor panel characterized by connecting the drain electrode of each thin film transistor arranged through each lobe by each pixel electrode corresponding to a data line and this data line.

[Translation done.]